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Office of Intellectual Property Counsel
3M Innovative Properties Company
PO Box 33427
St. Paul, Minnesota 55133-3427
651/733 1500

PATENT

Docket No.
52779USA1B

Transmittal of Continuing Patent Application - Rule 1.53(b)

Anticipated Classification

Box: Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Pursuant to 37 CFR 1.53(b), please file a

- ☐ continuation
- ☐ continuation-in-part
- ☒ divisional

application of pending prior Application No. 08/986,882, filed on December 8, 1997.

Inventor(s): Yu Chen, Joel A. Gerber, Brian E. Schreiber and Joshua W. Smith

Title: CIRCUIT ELEMENTS USING A Z-AXIS INTERCONNECT

1. ☒ Enclosed is a copy of the oath or declaration filed in the prior application.
2. ☐ Enclosed is a newly executed oath or declaration.
3. ☒ Enclosed is a copy of the specification as filed in the prior application.
4. ☐ Enclosed is a new specification.
5. ☐ Enclosed are sheet(s) of drawings.
6. ☒ The entire disclosure of the prior application is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein. (not applicable for CIP)
7. ☒ Please amend the specification by inserting before the first line the sentence:
   This is a divisional of Application No. 08/986,882, now allowed and filed on December 8, 1997.
8. ☐ Please cancel claims _____.
9. ☒ A preliminary amendment is enclosed.
10. ☐ This application is being filed by less than all the inventors named in the prior application. Please delete the names of the following person(s) who are not inventors of the invention being claimed in this application: _____

The fee for filing the application is computed as follows:

Claims As Filed, After Accounting For Any Claims Canceled Or Added In Paragraphs 8 Or 9 Above				
(1) For	(2) Number Filed	((3) Number Extra	(4) Rate	(5) Basic Fee $690
Total Claims	8 -20 =	0	x $18.	$0
Independent Claims	2 -3 =	0	x $78.	$0
Additional fee for filing one or more multiple dependent claims			$260.	$0
		Total Filing Fee Due →		$690

Transmittal of Continuing Application - Rule 1.53(b) (cont.)

Docket No. 52279USA B

11. ☒ Please charge to Deposit Account 13-3723 any fees under 37 CFR 1.16 and 1.17 which may be required to file and during the entire pendency of this application. This authorization includes the fee for any extension of time under 37 CFR 1.136(a) that may be necessary. To the extent any such extension should become necessary it is hereby requested. A copy of this transmittal letter for fee processing is enclosed.

12. An assignment
    - ☒ to 3M Innovative Properties Company is of record in the prior application.
    - ☐ from Minnesota Mining and Manufacturing Company to 3M Innovative Properties Company has been filed/is being filed concurrently in the prior application but is not yet recorded.
    - ☐ to is enclosed along with a completed Assignment Recordation Cover Sheet.

13. ☐ A power of attorney is enclosed.

14. ☒ Enclosed is a return receipt postcard.

15. ☐ Other

Respectfully submitted,

Registration Number	Telephone Number
39,766	512/984-3958
Date	
March 17, 2000	

Signature

Print Name

Matthew B. McNutt

Certificate of Express Mailing

Pursuant to 37 CFR 1.10 I certify that this application is being deposited on the date indicated below with the United States Postal Service "Express Mail Post Office to Addressee" service addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.

Express Mail Mailing Label No.	Signature of Person Mailing Application
EK243234238US	Linda Bradshaw
Date of Deposit	Printed Name of Person Mailing Application
March 20, 2000	Linda Bradshaw

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Docket No.: 52779USA1B

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Yu Chen, Joel Gerber, Brian Schreiber, and Joshua Smith	§	Group Art: Unknown
Serial No.: Not Assigned	§	Examiner: Not Assigned
Filed: March 20, 2000	§	
For: CIRCUIT ELEMENTS USING Z-AXIS INTERCONNECT	§	

PRELIMINARY AMENDMENT

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

This Preliminary Amendment accompanies the Divisional Application under 37 C.F.R. 1.53(b) filed herewith. With this Preliminary Amendment, claims 1-36 are cancelled. The cancelled claims were prosecuted in the parent application. Claims 37-43 are pending in the application.

Respectfully Submitted By:

Matthew B. McNutt
Registration No. 39,766

Date: March 20, 2000

Certificate of Mailing

☒ Pursuant to 37 CFR 1.8 I certify that this correspondence is being deposited on the date indicated below with the United States Postal Service as First Class Mail addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231 on **March 20, 2000.**

By: Linda Bradshaw
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PATENT APPLICATION

Docket No. 52779USA3A

METHOD FOR MAKING CIRCUIT ELEMENTS FOR A Z-AXIS INTERCONNECT

Field of the Invention

The present invention relates to circuits used in electronic packages. In particular, the invention relates to methods for preparing circuit elements that when bonded to other circuit elements form circuits with improved electrical and mechanical connections between adjacent circuit elements. The present invention additionally relates to circuits formed from the circuit elements prepared by the methods of the present invention.

Background of the Invention

Contemporary electronic devices require multiple circuit elements including, for example, integrated circuits, flexible circuits, single and multi-layer circuit boards, chip scale packages and ball grid array packages. These circuit elements must be connected by multiple precise mechanical and electrical connections in order for the devices to function reliably. Numerous approaches have been made to make reliable electrical connections in a low cost and efficient manner. These approaches have met with varying degrees of success.

One basic approach involves plated through hole (PTH) printed wiring board fabrication processes, for making the mechanical and elecfrical connections in separate processing steps. A typical mechanical connection between printed circuit boards is made by placing a sheet of adhesive resin impregnated fiber mat between two double sided printed circuit boards to form an assembly. This assembly is then placed in a lamination press and bonded under heat and pressure, mechanically connecting the boards.

Electrical connection then occurs in a separate series of steps, commonly known as a plated through hole (PTH) process. This PTH process typically includes drilling holes in the circuit board where electrical contact between layers

is desired, to create a via. These vias include walls that are cleaned and plated with conductive metallurgy.

However, this conventional PTH fabrication has several drawbacks. There are yield losses and reliability issues associated with the multiple step processing in PTH technology, resulting in increased costs as circuit feature size is reduced.

Processes that form the mechanical and electrical connections simultaneously potentially simplify the manufacturing process and reduce costs associated therewith. One method of simultaneously forming mechanical and electrical connections employs an adhesive ply with conductive buttons to attach circuit elements. For example, U.S. Patent No. 5,282,312 (DiStefano et al.) discloses two metal flexible circuits patterned with PTH vias. The connection between circuit layers is made by an adhesive bond ply with patterned conductive buttons. The buttons are placed in the bond ply at locations where connections are desired between the circuit layers. The adhesive bond ply has sufficient rigidity such that conduction through the bond ply is only permitted at conductive buttons. One drawback to this construction is the required complex patterning process and subsequent registration of the bond ply to the circuit layers, that adds cost and decreases yield.

Another approach to making circuit element connections, such as those between chips and boards, flexible circuits to boards and other related circuit structures, and also to form inter-layer connections in circuit boards, involves making the mechanical and electrical connections simultaneously in one press step or a series of steps. An example of this approach involves using anisotropic or z-axis adhesives, a recently developed class of conductive adhesives, to replace solder for surface mounting. These anisotropic adhesives include adhesive films loaded with conductive particles at a much lower volume fraction than conventional isotropically conductive adhesives.

In operation, when pressed between conductors of circuit elements, the anisotropic adhesive film is compressed, such that the adhesive is forced out of the way of the conductors, while the conductive particles remain trapped between the conductors, forming electrical contacts therebetween. It is important for these

anisotropic adhesive films to have a conductive particle loading that is sufficiently disperse to prevent particle shorting in the plane of the circuit.

U.S. Patent No. 5,502,884 (Casson et al.) discloses a method for fabricating a multilayer circuit board, that uses an anisotropically conducting adhesive to connect multiple layers of double sided circuitry. However, the resultant circuit has drawbacks, in that the use of a random dispersion of particles can not provide the high density of hole (or via) interconnections required for high performance circuits due to the possible electrical shorting between contacts. In addition, the random dispersion of particles requires patterned masking of the circuit layers to prevent shorting between layers.

Circuit elements have also been connected with nonconducting adhesives, by using patterned bumps on the circuit elements. For example, U.S. Patent No. 4,749,120 (Hatada) describes a mechanical connection between a semiconductor device having an array of conducting bumps and corresponding pads on a wiring board, with a nonconducting adhesive. During the bonding process, the bumps are forced through the adhesive, making electrical contact with their respective pads.

U.S. Patent No. 5,401,913 (Gerber et al.) discloses multiple circuit layers having columns (bumps) of a metal. The circuit layers are mechanically connected by a nonconducting adhesive layer placed between each successive circuit layer. The circuit layers are subsequently laminated in the presence of heat and pressure, such that the bumps are forced through the adhesive layer and contact their respective pads on the adjacent circuit layer.

For many of the above described interconnection techniques, it is requisite that the respective conducting particles or bumps penetrate the adhesive layer, in order to form an electrical connection between conductive members of the circuit elements. This requirement puts significant constraints on the selection of adhesives. For example, insufficient flow can result in trapping small amounts of adhesive between the conducting elements, resulting in high resistance bonds and/or environmentally unstable bonds. Alternately, too much flow of the adhesive typically results in adhesive deposits in undesired locations on the circuit

elements or resultant circuit as well as bond line nonuniformity, detrimental to electrical performance. Excess adhesive flow can also starve regions in the bond of adhesive, resulting in voiding or regions of very thin bond lines, leading to reduced adhesion and poor environmental performance.

Summary of the Invention

The present invention advances the art by providing methods for mass producing circuit elements having adhesive in single or multiple layers, and substantially uniform conducting bumps, for making Z-axis electrical connections between multiple circuit elements, two or more of these elements being joined to form multi-layered circuits. In accordance with the principles of the present invention, such circuit elements can be economically mass produced by providing a substrate having a plurality of conductive bumps, covering the substrate and the conductive bumps with an insulating layer including adhesive, and selectively removing a portion of the insulating layer to expose at least the apexes of the bumps. After the portion of the insulating layer has been removed, it is significant that a sufficient amount of the insulating layer remains on the substrate for facilitating mechanical connections between the circuit element and a second circuit element. The resultant circuit element produced in accordance with the present invention, upon its being joined to a corresponding circuit element or layer, provides for highly reliable electrical connections of good electrical conductivity between bumps and their corresponding pads.

The present invention teaches a method for making electronic circuit elements that includes the steps of initially providing a precursor element with a first insulating layer and a first conductor attached to said first insulating layer. The first insulating layer has a first surface, at least a portion of which defines a first surface plane. The precursor element has a surface including the first surface of the insulating layer. An electrically conducting member, or bump, is then placed onto the precursor circuit element into electrical communication with the first conductor. The bump extends such that its apex is beyond the first surface plane. Additionally, the precursor element surface and the conducting member surface define a major surface of a

predetermined shape. A second insulating layer is then placed (e.g., by standard deposition techniques) onto substantially all of the major surface. This second insulating layer includes oppositely disposed portions extending laterally from the bump, these oppositely disposed portions extend to points below the apex, of the bump or electrically conducting member. At least a portion of the second insulating layer proximate the apex of the bump or electrically conducting member is subsequently removed.

This now completed circuit element may be aligned with a correspondingly configured circuit element or circuit layer. The circuit element and correspondingly configured circuit element or circuit layer are brought together and joined, such that electrical connections between their conducting components have been made. This process can be used as desired on as many circuit elements and/or circuit layers as necessary to produce the desired multi-layered circuit.

Brief Description of the Drawings

The present invention will be described with reference to the accompanying drawings, wherein like reference numerals identify corresponding or like components.

In the Drawings:

FIGs. 1a-1d are cross sectional views of a first method of the present invention;

FIG. 2 is a top view of the precursor circuit element of FIG. 1a;

FIGs. 3a-3c and 4a-4c are cross sectional views of alternate insulating layer removal methods, shown in use with the method of FIGs. 1a-1d;

FIGs. 5a-5f are cross sectional views of a second method of the present invention;

FIGs. 6a-6c are micrographs of circuit elements at various stages of processing in accordance with the present invention; and

FIG. 7 is a chart of electrical resistance distribution between an unpolished control and a circuit element made in accordance with the present invention.

Detailed Description of the Drawings

The present invention, embodiments of which are described below and illustrated in the figures, relates generally to methods for preparing a circuit element and electrically interconnecting two or more circuit elements to form a multi-layered circuit. In the exemplary circuits described below, at least one circuit layer includes a circuit element prepared in accordance with the present invention.

As used throughout this application "circuit elements" refers generally to substrates of dielectric or other equivalent materials that support a circuit network having single or multiple layers of conductive traces, pads or other electrically conducting pathways. The dielectrics employed may be either rigid or flexible (non-rigid), and formed of single or multiple layers. Some typical circuit elements include flexible circuits, printed circuit boards, integrated circuits (packaged and unpackaged), including chips, dies and combinations thereof, and other similar components. These circuit elements, when combined with each other, similar components, or additional structures, form circuits, or multi-layered circuits.

In accordance with the present invention, only one or two electrical connections between two circuit elements are shown in FIGs. 1a-1d and 5a-5f, each circuit element having a single conductive circuit trace layer (but could also have multiple conductive circuit traces). These interconnections between two circuit elements are exemplary only, for purposes of illustrating the present invention, as the present invention typically involves multiple circuit elements of single or multiple circuit layers, with multiple conducting members (FIGs. 3a-3c), for multiple electrical connections between multiple adjacent circuit elements (and other similar structures) in order to form multi-layered circuits.

In FIGs. 1a-1d, there is detailed a first method for preparing a circuit element 20 (FIGs. 1c and 1d) that is joined with a second circuit element 21 to form a multi-layered circuit. The circuit element 20 is initially formed from a precursor circuit element 20p.

Turning to Fig. 1a, the precursor circuit element 20p (that is ultimately processed into the first circuit elements 20, 20', 20''), and second circuit element

21 are typically formed of substrates 22, 23 of a dielectric, such as a polyimide foil. These substrates 22, 23 preferably have substantially planar surfaces 22a, 23a, and include single or multiple conductive circuit traces of an electrically conductive material such as copper or the like (not shown), in electrical communication with pads 24, 25 on the substrates 22, 23.

These pads 24, 25 may be portions of one or more of the conductive circuit traces, or may be separate conductive members of the circuit elements 20, 21 (or the precursor circuit element 20p) in electrical communication with one or more of the conductive circuit traces. The pads are typically of an electrically conductive material, such as copper or the like, that protrude from the respective surfaces 22a, 23a, and are placed onto the respective substrates 22, 23 at their surfaces 22a, 23a, by methods such as electrodeposition or vapor deposition. Alternately, the pads 24, 25 could be placed into their respective substrates 22, 23, such that they are flush with their respective substrate surfaces 22a, 23a, or below the plane of their respective substrate surfaces 22a, 23a. Alternatively, for some circuit elements, such as chips in integrated circuits, there would be input/output pads that are generally recessed slightly with respect to a passivation layer on the substrate.

The precursor circuit element 20p includes electrically conducting members, preferably in the form of "bumps" 30, in electrical contact with at least one pad 24, although contact of a single bump with multiple pads is also permissible. These bumps 30 preferably have a substantially spherical-shaped portion 31 with a surface 30a, and protrude from the pads 24 to an apex 32 along the bump surface 30a. Other shapes, or portions thereof, such as rectangular, square, oval, triangular, pentagonal, polygonal, toroidal, annular ring, other ring-like shape, etc., and combinations thereof are also permissible for the bumps 30.

It is preferred that the height and shape of the bumps 30 be substantially uniform, to enable the bumps to make sufficient electrical contact(s), as described below. The surface 30a of the bumps 30, along with the substrate surface 22a, and the surfaces of the pads 24 not covered by the bumps 30, forms a structured or major surface 33 of the precursor circuit element 20p.

The bumps 30 are made of electrically conductive material(s), preferably as metals, but could also be electrically conductive adhesives, deposited onto the substrate surface 22a by conventional deposition techniques. Metals for the bump 30 include tin, aluminum, indium, lead, gold, silver, bismuth, copper, palladium, and the like and alloys of these materials. These metals forming the bump 30 also render it heat conductive, so the resultant circuit element can be used as a heat sink. For example, a circuit element of the present invention could be attached to a chip, to allow heat to be dissipated from the chip through the bumps 30.

The pads 25 on the second circuit element 21 are preferably located on the substrate 23 of the second circuit element 21 at positions corresponding to those of the bumps 30 on the precursor circuit element 20p, so that, when registered together as matched elements the bumps and pads will be centered on each other for good contact. In accordance with the present invention, the first circuit element 20 may also include pads on its substrate surface 22b opposite the substrate surface 22a having the bumps 30. Additionally, the second circuit element 21, may include bumps (in accordance with those described above) on pads on its substrate surface 23b, as well as bumps (in accordance with those described above) on the pads 25 (to be used in forming a bump-to-bump contact in the resultant circuit), to be part of a multi-layered circuit. The placement of these additional pads or bumps on the precursor circuit element 20p and second circuit element 21 (and additional circuit elements if desired) is dependent upon the number of circuit layers desired for the particular circuit being designed.

An insulating layer 36, preferably an adhesive, may include additional components known to those skilled in the art, such as, for example, inorganic fillers and the like. The layer 36 is placed on the precursor circuit element 20p by techniques such as, for example, solution coating, sheet laminating, or spraying. Suitable adhesives include heat-flowable, thermosetting or thermoplastic adhesives, either alone or in combinations thereof. Examples of such adhesives include epoxies, cyanate esters, acrylates, phenolics, silicones, polyimides, polyamides and the like. These adhesives facilitate bonding between the circuit elements 20, 21 (FIG. 1d)

The insulating layer 36 is deposited onto the precursor circuit element 20p in substantial conformance with the topography of the major surface 33, such that the surfaces 36a of the insulating layer 36, extending laterally from the bumps 30, do not extend beyond the apex 32 of the bump 30. Preferably, the insulating layer 36 deposited onto the precursor circuit element 20p has a substantially uniform thickness. The deposited insulating layer 36 should conform to the topography of the major surface 33. Additionally, the surfaces 36a of the insulating layer 36 that extend laterally from the bumps 30 define a surface A (See FIG. 1b). Fig. 2 shows a plane view of the circuit element 20 from the bump 30 side.

As shown in FIGs. 1b and 1c, the precursor circuit element 20p is further processed by removing at least a portion of the insulating layer 36. The layer 36 is preferably removed in the area between plane A and the apexes 32 of the bumps 30 to expose a portion of each bump 30. This removal of at least a portion of the insulating layer 36 may also involve removing a portion of each bump, with any removed portions of the bumps preferably limited to the area between plane A and the apexes 32 of the bumps 30. As a result of this preferred removal, portions of the bumps 30 remain covered with the insulating layer 36. The amount of the insulating layer 36 that is removed should be sufficient to expose the material of the bump 30 at the bump apex 32 (top), such that a sufficient electrical contact can be made between the bump 30 and its respective pad 25 (when the circuit elements 20, 21, are joined or laminated together, as shown in FIG. 1d and described below). A sufficient amount of the insulating layer 36 should remain to facilitate a sufficient mechanical connection or bond when the circuit elements 20, 21 (FIG. 1d), are joined or laminated together.

Preferably, removal of the insulating layer 36 (and portions of the bumps 30, if necessary) should be limited to the area proximate the apexes 32 of the bumps 30, at points substantially beyond plane A. Only small amounts of the insulating layer 36 should be removed during this process, so that a sufficient portion of the insulating layer 36, remains on the bump and substrate of the circuit element 20 (FIG. 1c) for facilitating a sufficient mechanical connection when the circuit elements 20,21 are joined (FIG. 1d).

A first method, as detailed in FIGs. 1b, for removing the insulating layer 36, to produce the (first) circuit element 20 (FIG. 1c) with at least a portion of the bumps 30 exposed, is by mechanical processes including abrasion (or cleaning). In this method, the portions of the insulating layer 36, extending beyond plane A (toward the apexes 32 of the bumps 30) are then contacted with an abrasive material 40, such as sand paper of approximately 120-1200 grit or other suitable abrasive materials, including microabrasives such as, for example, those available under the trade designation Imperial Lapping Film from 3M Co., St. Paul, Minnesota. The abrasive material should remove sufficient material of the insulating layer 36 and the bumps 30 to expose at least a portion of the material of the bumps 30. Preferably, abrasion should not extend further than plane A (toward the substrate 22), and should preferably be in an area proximate to the apexes 32 of the bumps 30. This way, the resultant circuit element 20, shown in FIG. 1c, has a newly exposed bump surface 30b, beyond plane A, and there remains a sufficient amount of material of the insulating layer 36 on the substrate 22 and the bump to facilitate the mechanical connection between the circuit elements 20, 21 (FIG. 1d). Preferably, a substantial portion of the insulating layer 36 remains intact, having been unaffected by this removal step.

The first abrasion removal method (with abrasive material 40) is preferred when bump height is non-uniform (although uniformity in bump height is preferred). By removing a portion of the bump 30, as occurs with this abrasion removal method, variations in bump height and shape can be corrected.

A second removal method, as an alternate to the abrasion method detailed above, is shown in FIGs. 3a-3c. This alternate method allows for removal of a sufficient portion of the insulating layer 36, to expose the material of the bumps 30, by bringing a smooth surfaced article 60 or smooth surfaced roller (not shown), with a substantially planar surface 61, into contact with the precursor circuit element 20p (in the direction of arrows 62), preferably beyond plane A (in a direction toward the apexes 32 of the bumps 30) (FIG. 3a). The article 60 and specifically, its surface 61 subsequently is pushed into contact with the insulating layer 36 on the precursor circuit element 20p toward the bumps 30. This pushing

action (in the direction of the arrows 62), forces the adhesive of the insulating layer 36 away from the apexes 32 of the bumps 30 (in the direction of the arrows 64), by thinning and/or cracking the adhesive of the insulating layer 36, as shown specifically in FIG. 3b. In an optional step, heat may be applied to aid the flow of the adhesive of the insulating layer 36.

The planar surfaced article 60 does not adhere to the adhesive of the insulating layer 36. As shown in FIG. 3c, as the planar surfaced article 60 is removed from contact with the precursor circuit element 20p (in the direction of arrows 66), the resultant circuit element 20' has an exposed portion of the surface 30a of the bumps 30 (sufficient for a subsequent electrical connection), that is proximate the apexes 32 of the bumps 30. Additionally, sufficient amounts of the material (e.g., adhesive) insulating layer 36 remain on the substrate 22 and the bump 30 of the circuit element 20' to facilitate the mechanical connection between the circuit elements 20', 21. Preferably, a sufficient amount of the insulating layer 36 remains intact, having been unaffected by this removal step. The circuit element 20' is ready for further processing, in accordance with the methods as detailed below (as described below for circuit element 20).

In another alternate removal method, shown in FIGs. 4a-4c, an article 80 with a surface 81 (exaggerated for illustration purposes) having an affinity for the material (e.g., adhesive) of the insulating layer 36, greater than the surfaces 30a of the bumps 30, is brought into contact with the precursor circuit element 20p (in the direction of the arrows 82) (FIG. 4a). It is preferred that the surface 81 be substantially planar and that this surface be rough or sticky. The article 80 is subsequently pushed into contact with the insulating layer 36 of the precursor circuit element 20p toward the bumps 30 (in the direction of the arrows 82), such that only the insulating layer 36, along the apexes 32 of the bumps 30 (preferably along an arc proximate the apex 32) beyond plane A, contacts the article surface 81 (FIG. 4b).

As shown in FIG. 4c, upon removal (separation) of the article 80 from the precursor circuit element 20p (now the circuit element 20'')(in the direction of the arrows 84), the insulating layer portions 36', formerly on the precursor circuit

element 20p, are now on the article surface 81. With the insulating layer portions 36' removed, the resultant circuit element 20'' has a now-exposed bump surface 30a proximate the bump apexes 32. This exposed bump surface 30a is sufficient to promote an electrical connection between this circuit element 20" and another circuit element (e.g., circuit element 21), while substantial amounts of the insulating layer 36 remain on the substrate 22 and bump 30 to facilitate the mechanical connection between the above circuit elements. Preferably a sufficient amount of the remaining insulating layer 36 remains intact, having been unaffected by this removal step. Upon completion of the removal step, the circuit element 20'' is ready for further processing, in accordance with the methods as detailed below (as described below for circuit element 20).

In another alternate step (not shown), the insulating layer 36 at the apexes 32 of the bumps 30 is thinned by first pushing the precursor circuit element 24 against a surface, such as the surface of a hot roller. This action pushes the material, e.g., adhesive, of the insulating layer 36 away from the apexes 32 of the respective bumps 30, such that the insulating layer 36 remaining on the apexes 32 of the bumps 30 is thinned substantially. This remaining thinned adhesive is removed by etching techniques, such as, for example, reactive ion etching, plasma etching, laser ablation, corona treatment and/or combinations thereof. The etching step is controlled to terminate when the thinned insulating layer 36 at the apexes 32 of the bumps 30 has been removed, while the bulk of the insulating layer 36 along the sides of the bumps 30 and the substrate 22 remains in an amount sufficient to facilitate the mechanical connection between the circuit elements. Preferably, these areas of the insulating layer 36, remain intact, having been substantially unaffected by the etch process. The newly-prepared circuit element is ready for further processing in accordance with the methods detailed below (as described below for circuit element 20).

Once a sufficient portion of the bump 30 is exposed, by any of the above described removal methods, or combinations thereof, the now complete circuit element 20, 20', 20'' may be joined with another circuit element, e.g., the second circuit element 21, for producing a multi-layered circuit. While only the joining of

the circuit element 20 produced by abrasion, to a second circuit element 21, is detailed below, other circuit elements 20', 20'' (and those not shown), produced by the alternate methods detailed above, could be joined to the second circuit element 21 in accordance with the method steps detailed below.

The now complete first circuit element 20, produced by abrasion method with the abrasive material 40 (above), results in bumps 30 with newly exposed surfaces 30b, as shown in FIG. 1c. This circuit element 20 is subsequently aligned with the second circuit element 21, and these circuit elements 20, 21 are brought together. Specifically, the bumps 30 are aligned with their corresponding pads 25 on the second circuit element 21. The alignment can be performed by any suitable conventional alignment technique, such as mechanical alignment using alignment pins, optical registration using fiducials and other methods known in the art.

The circuit elements 20, 21 are joined or laminated as pressure is applied to them, making simultaneous mechanical and electrical connections therebetween. An optional heating step, e.g., to assist in flowing or curing the adhesive of the insulating layer 36 (if a flowable adhesive is used), may be done at any time during the lamination process, for as long as desired. The circuit elements 20, 21 are now bonded together into an intermediate circuit 46 (multi-layered circuit), as shown in FIG. 1d. The adhesive of the insulating layer 36 provides the mechanical strength to the intermediate circuit 46 and the exposed bumps 30 are in physical contact with their respective corresponding pads 25, creating the electrical connection.

Turning now to FIGs. 5a-5f, there is detailed a second method for preparing a circuit element 120 (FIGs. 5d-5f), from a precursor circuit element 120p and joining it with a second circuit element 121 (FIGs. 5e and 5f) to form a circuit, in accordance with the methods described above. The precursor circuit element 120p (that is ultimately processed into the circuit element 120) and the circuit element 121 are formed of substrates 122, 123 comprised of materials such as polyimide films (as described above). The substrates 122, 123 preferably have surfaces 122a, 122b, 123a, 123b, with substantially planar surfaces 122b and 123a having pads 124, 125 protruding therefrom. The pads 124, 125 are of the

materials, and are constructed and arranged with respect to the substrates 122, 123, in accordance with the arrangements described above. The pads 124, 125 are in electrical communication with single or multiple conductive circuit traces (not shown) and, similar to the pads 24, 25 above (see FIGs. 1a-1d), may be portions of one or more of the conductive circuit traces.

In FIG. 5b, a hole (via) 126, is then made in the substrate 122, of the precursor circuit element 120p, preferably by wet milling or dry milling techniques. Wet milling techniques may include, chemical etching and the like while dry milling techniques may include laser ablation, ion milling, reactive ion etching and the like. This hole 126 in the substrate 122 extends to the pad 124 and may be formed into any shape (round, square, rectangular, triangular, ovular, etc.). The walls 128 (having surfaces 128a) of the hole (via) 126, preferably extend outward from the pad 124.

Electrically conducting material, preferably in the form of bumps 130 (of the materials and of the shapes described above) is deposited, in accordance with the methods described above, into the vias 126. While only a single bump 130 is shown, the singular and plural of the term "bump" is used interchangeably throughout the description of these drawing figures, for as discussed above, the present invention involves multiple bumps (see FIG. 2 and the Examples below) in forming the multiple circuit interconnects. The bumps 130 could be arranged on the precursor circuit element 120p (circuit element 120) and second circuit element 121 in accordance with any of the arrangements detailed above.

These bumps 130 preferably have a substantially spherical-shaped portion 131 with a surface 130a, and protrude from the pads 124 to an apex 132 along the bump surface 130a. This 132 apex preferably extends to a point beyond a plane B (defined by the surfaces 136a of the insulating layer 136 extending laterally from the bumps 130), in order that portions of the insulating layer 136 or portions of the insulating layer 136 and the bump 130 can be removed at a point at or beyond, preferably beyond, plane B (detailed below and in FIG. 5c), to expose a portion of the bump 130 for subsequent electrical connection of the bump 130 of the circuit element 120, with a corresponding pad 125 on the opposite circuit element 121.

As detailed above, it is preferred that the height and shape of the bumps 130 be substantially uniform, to enable the bumps 130 to make sufficient electrical contact(s), as described below. The surface 130a of the bumps 130, along with the substrate surface 122a, the via wall surfaces 128a and the surfaces of the pads 124, not covered by the bumps 130, forms a structured or major surface 133 of the precursor circuit element 120p.

An insulating layer 136, in accordance with that described above, is deposited onto the precursor circuit element 120p, in accordance with the techniques described above, in substantial conformance with the topography of the major surface 133, such that the surfaces 136a of the insulating layer 136, extending laterally from the bumps 130, do not extend beyond the apex 132 of the bump 130. Preferably, the insulating layer 136 is deposited onto the precursor circuit element 120p, to be of a substantially uniform thickness, this deposition being such that the deposited insulating layer 136 takes a shape that conforms to the topography of the major surface 133.

As shown in FIG. 5c, the precursor circuit element is further processed as a portion of the insulating layer 136 and a portion of the bump 130 are removed as an abrasive material 140, similar to that discussed above, is moved in the direction of the arrow 142 into contact with the insulating layer 136 and the bump 130, at a point beyond plane B, proximate the apex 132 of the bump 130, in accordance with the abrasion removal process detailed above (and shown in FIG. 1b). Alternately, removal processes in accordance with the alternate (three) additional removal methods discussed above (two of the methods detailed in FIGs. 3a-3c and 4a-4c) are also permissible. Similar to that described above, it is preferred that removal of the insulating layer 136 (and portions of the bump 130 if necessary such as with the abrasion method) should be such that a sufficient amount of the bump 130 is exposed for making a sufficient electrical contact (with the corresponding pad 125 of the circuit element 121), and that there remains a sufficient amount of the insulating layer for facilitating a sufficient mechanical connection (bond) when the circuit elements 120, 121 are joined or laminated together (FIGs. 5e and 5f).

Upon completion of the abrasion step, the resultant circuit element 120, as shown in FIG. 5d, has bumps 130 with newly exposed surfaces 130b at or beyond, preferably beyond, plane B (away from the substrate 122). A sufficient amount of the insulating layer 136 remains for a mechanical connection of circuit elements 120, 121. Preferably, as described above, the insulating layer 136 remains substantially intact, having not been substantially affected by this removal step.

As shown in FIG. 5e, the now complete first circuit element 120 is aligned with the second circuit element 121, and these circuit elements 120, 121 are brought together. Specifically, the bumps 130 are aligned with their corresponding pads 125 on the second, now adjacent, circuit element 121. The alignment can be performed by any suitable conventional alignment technique, such as mechanical alignment using alignment pins, optical registration using fiducials and other methods known in the art.

The circuit elements 120, 121 are joined or laminated as pressure is applied to them, making simultaneous mechanical and electrical connections therebetween. An optional heating step, e.g., to assist in flowing or curing the adhesive of the insulating layer 136 (if a flowable adhesive is used), may be done at any time during the lamination process, for as long as desired. The circuit elements 120, 121 are now bonded together into an intermediate circuit 146 (multi-layered circuit), as shown in FIG. 5f. The adhesive of the insulating layer 136 provides the mechanical strength to the intermediate circuit 146 and the exposed bumps 130 are in physical contact with their respective corresponding-pads 125, creating the electrical connection.

EXAMPLE 1

A patterned flexible circuit was made in accordance with FIGs. 5a-5f. The circuit elements included polyimide dielectric films with patterned copper traces on one side. At least one of the circuit elements included holes (vias) on the side opposite the patterned circuit traces. The patterned traces and holes were made by conventional methods. The vias were located at points where electrical

connections were desired. Bumps of solder were created by deposition. The resultant bumps, as shown in the SEM micrograph at FIG. 6a, extended to a height of about 50 micrometers and protruded above the plane formed by the polyimide dielectric film surface.

A layer of adhesive, available under the trade designation PYRALUX LF from E. I. DuPont de Nemours, Inc., Wilmington, Delaware, USA, was applied to the surface of the circuit element including the bumps with a hot roll laminator at 120°C, at a substantially uniform thickness of approximately 25 micrometers. The resultant circuit element is shown in an SEM micrograph at FIG. 6b. Abrasives were used separately to remove the adhesive from areas proximate the apexes of the bumps as described above. These abrasives included 600 grit sandpaper, available under the trade designation SCOTCHBRITE (5S-Fine), from 3M Co., St. Paul, Minnesota, USA, as well as microabrasives available under the trade designation Imperial Lapping Film from 3M Co., St. Paul, Minnesota, USA. The circuit with adhesive layer, removed by the 3M Imperial Lapping film microabrasive, is shown in the SEM micrograph of FIG. 6c.

Two circuit elements of the above disclosed dielectric films were stacked on top of each other using a metal plate mounted with pins for registration of the films, and the entire assembly was placed in a platen press and laminated at 170°C at 450 psi (3.2×10^6 N/m^2) for 30-90 minutes. The completed circuit interconnect assembly was removed from the press.

A control was made in the manner identical to the above sample, except that the abrasive steps were omitted, so as not to remove the adhesive layer from the apexes of the bumps.

FIG. 7 shows a comparison of the electrical resistance distribution for 175 vias between the sample circuit element with abraded or "polished" bumps (the electrical resistance illustrated by line 180) and a control sample with 175 vias of unabraded or "unpolished" bumps (the electrical resistance illustrated by line 181). Based on these results, a two order of magnitude difference in electrical resistance was observed.

While embodiments of the present invention have been described so as to enable one skilled in the art to practice the techniques of the present invention, the preceding description is intended to be exemplary. It should not be used to limit the scope of the invention, which should be determined by reference to the following claims.

What is claimed is:

1. A method for making an electronic circuit comprising:

providing a first circuit element, said first circuit element made by steps including:

providing a precursor element including a first insulating layer and a first conductor attached to said first insulating layer, said first insulating layer having a first surface, at least a portion of said first surface defining a first surface plane and said precursor element having a surface, said precursor element surface including said first surface of said insulating layer;

placing a conducting member onto said precursor circuit element into electrical communication with said first conductor, said conducting member including a surface and protruding to an apex at a first level, said first level at least beyond said first surface plane;

said precursor element surface and said conducting member surface defining a major surface of a predetermined shape;

placing a second insulating layer onto substantially all of said major surface, said second insulating layer including oppositely disposed portions extending laterally from said conducting member along said first surface of said first insulating layer, said second insulating layer at said oppositely disposed portions extending to a second level, said first level beyond said second level;

removing at least a portion of said second insulating layer proximate said apex of said conducting member;

providing a second circuit element with a second conductor;

aligning said first circuit element with said second circuit element; and

applying pressure to said first and second circuit elements, to join said circuit elements, such that said conducting member provides

electrical conduction between said first conductor and said second conductor.

2. The method of claim 1, wherein said precursor circuit element and said second circuit element each include at least one dielectric film.

3. The method of claim 2, wherein said first insulating layer includes said at least one dielectric film.

4. The method of claim 1, wherein said conducting member includes a metal bump.

5. The method of claim 4, wherein said step of providing said precursor circuit element additionally comprises forming a via in said precursor element in said first insulating layer proximate said first conductor.

6. The method of claim 1, wherein the second insulating layer is placed onto said major surface in a substantially uniform thickness and in conformance with said predetermined shape of said major surface.

7. The method of claim 6, wherein said oppositely disposed portions of said second insulating layer include surfaces, at least a portion of each of said second insulating layer surfaces defining a second surface plane, and said removal additionally includes removing at least a portion of said second insulating layer beyond said second surface plane.

8. The method of claim 1, wherein said second insulating layer includes at least one adhesive.

9. The method of claim 8, wherein said at least one adhesive is a heat-flowable adhesive.

10. The method of claim 1, further comprising, applying heat to said first and second circuit elements.

11. The method of claim 10, wherein said step of applying heat includes heating said first and second circuit elements to slightly less than the melting temperature of said conducting member.

12. The method of claim 1, wherein said first conductor and said second conductor include copper.

13. The method of claim 1, wherein the step of placing the conducting member onto said precursor element includes deposition of a metal.

14. The method of claim 7, wherein said removal includes contacting said second insulating layer with an abrasive material.

15. The method of claim 14, wherein said abrasive material is a microabrasive.

16. The method of claim 7, wherein said removal includes placing an article into contact with said second insulating layer proximate said apex, applying pressure to said pressure element, and releasing said pressure.

17. The method of claim 16, wherein said step of releasing said pressure includes removing said article from contact with said ~~pressure~~ element.

18. The method of claim 16, wherein said article has substantial affinity for the material of the second insulating layer, whereby releasing said pressure includes separating said article from said precursor circuit element, wherein at least portions of the second insulating layer proximate said apex are removed and remain on said article.

19. The method of claim 16, additionally comprising etching said second insulating layer proximate said apex.

20. A method for making an electronic circuit element comprising:

providing a precursor element including a first insulating layer and a first conductor attached to said first insulating layer, said first insulating layer having a first surface, at least a portion of said first surface defining a first surface plane and said precursor element having a surface, said precursor element surface including said first surface of said insulating layer;

placing a conducting member onto the precursor circuit element into electrical communication with said first conductor, said conducting member including a surface and protruding to an apex at a first level, said first level at least beyond said first surface plane;

said precursor element surface and said conducting member surface defining a major surface of a predetermined shape;

placing a second insulating layer onto substantially all of said major surface, said second insulating layer including oppositely disposed portions extending laterally from said conducting member along said first surface of said first insulating layer, said second insulating layer at said oppositely disposed portions extending to a second level, said first level beyond said second level; and

removing at least a portion of said second insulating layer proximate the apex of said conducting member.

21. The method of claim 20, wherein said precursor circuit element and said second circuit element each include at least one dielectric film.

22. The method of claim 21, wherein said first insulating layer includes said at least one dielectric film.

23. The method of claim 20, wherein said conducting member includes a metal bump.

24. The method of claim 23, wherein said step of providing said precursor circuit element additionally comprises forming a via in said precursor element in said first insulating layer proximate said first conductor.

25. The method of claim 20, wherein the second insulating layer is placed onto said major surface in a substantially uniform thickness and in conformance with said predetermined shape of said major surface.

26. The method of claim 25, wherein said oppositely disposed portions of said second insulating layer include surfaces, at least a portion of each of said second insulating layer surfaces defining a second surface plane, and said removal additionally includes removing at least a portion of said second insulating layer beyond said second surface plane.

27. The method of claim 20, wherein said second insulating layer includes at least one adhesive.

28. The method of claim 27, wherein said at least one adhesive is a heat-flowable adhesive.

29. The method of claim 20, wherein said first conductor includes copper.

30. The method of claim 20, wherein the step of placing the conducting member onto said precursor element includes deposition of a metal.

31. The method of claim 26 wherein said removal includes contacting said second insulating layer with an abrasive material.

32. The method of claim 31, wherein said abrasive material includes a microabrasive.

33. The method of claim 26, wherein said removal includes placing an article into contact with said second insulating layer proximate said apex, applying pressure to said precursor element, and releasing said pressure.

34. The method of claim 33, wherein said step of releasing said pressure includes removing said article from contact with said precursor circuit element.

35. The method of claim 33, wherein said article has substantial affinity for the material of the second insulating layer, whereby upon separation of said article from said precursor circuit element, at least a portion of the second insulating layer proximate said apex is removed.

36. The method of claim 31, additionally comprising etching said second insulating layer proximate said apex.

37. An electronic circuit element made in by the method comprising:

providing a precursor element including a first insulating layer and a first conductor attached to said first insulating layer, said first insulating layer having a first surface, at least a portion of said first surface defining a first surface plane and said precursor element having a surface, said precursor element surface including said first surface of said insulating layer;

placing a conducting member onto the precursor circuit element into electrical communication with said first conductor, said conducting member including a surface and protruding to an apex at a first level, said first level at least beyond said first surface plane;

said precursor element surface and said conducting member surface defining a major surface of a predetermined shape;

placing a second insulating layer onto substantially all of said major surface, said second insulating layer including oppositely disposed portions extending laterally from said conducting member along said first surface of said insulating layer, said second insulating layer at said oppositely disposed portions extending to a second level, said first level beyond said second level; and

removing at least a portion of said second insulating layer proximate the apex of said conducting member.

38. An electronic circuit element comprising:

a first insulating layer having at least one surface, at least a portion of said surface defining a first surface plane;

at least one conductor along at least a portion of said at least one surface,

a conducting member in communication with said at least one conductor, said conducting member protruding to an apex at a first level, said first level beyond said first surface plane, said conducting member including a surface, said surface of said first insulating layer, said at least one surface of said conductor, and said surface of said conducting member, defining a major surface of a predetermined shape;

a second insulating layer along at least a portion of said major surface whereby at least a portion of said conducting member remains exposed, said second insulating layer including portions extending laterally from said conducting member along said first insulating layer, said laterally extending portions extending from said first surface plane to a second level, said second level less than said first level.

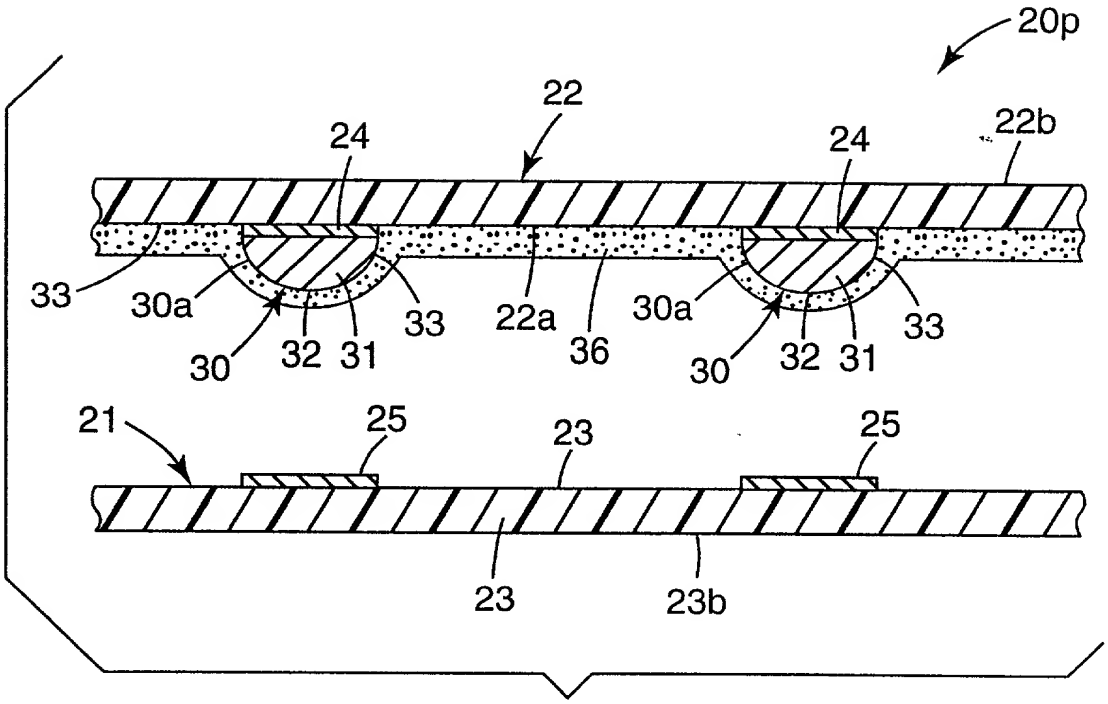
39. The circuit element of claim 38, wherein said exposed portion of said conducting member is proximate said apex.

40. The circuit element of claim 39, wherein said exposed portion of said conducting member, includes said surface of said conducting member.

METHOD FOR MAKING CIRCUIT ELEMENTS FOR A Z-AXIS INTERCONNECT

ABSTRACT

Methods for producing circuit elements the resultant circuit elements, and methods for making circuits therefrom are disclosed. A precursor circuit element includes a first insulating layer with conductor thereon and an electrically conducting member or bump, protruding from the conductor, that provide a shape to one surface of the precursor circuit element. A second insulating layer, including an adhesive, is placed onto the precursor circuit element and assumes the shape of the aforementioned surface of the precursor circuit element. A portion of the insulating layer is removed proximate the apex of the bump to expose at least a portion of the bump, for a sufficient electrical connection with a subsequent circuit element, while maintaining a sufficient amount of the insulating layer on the first initiating layer and bump to facilitate the mechanical connection (bond) between this resultant circuit element and a second circuit element, that may or may not have been produced by the method of the present invention.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23b

Fig. 1a

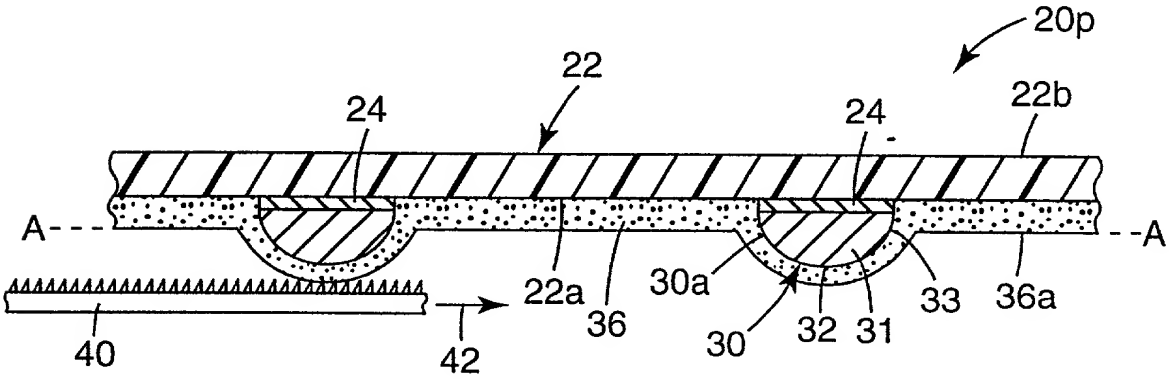
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Fig. 1b

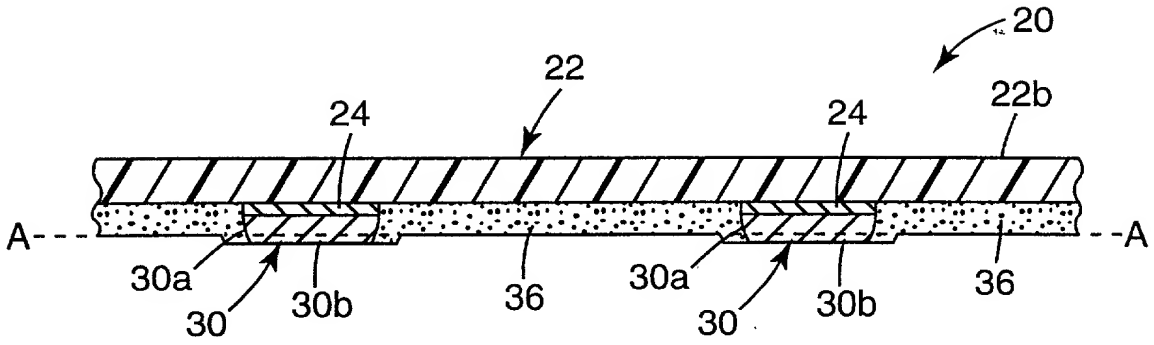
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Fig. 1c

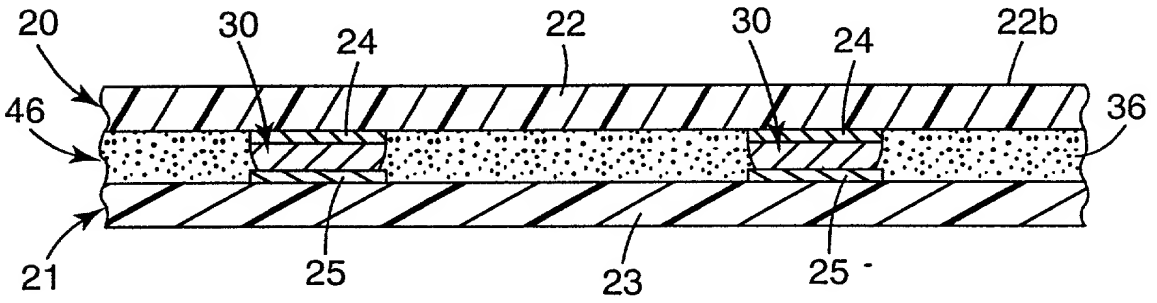
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Fig. 1d

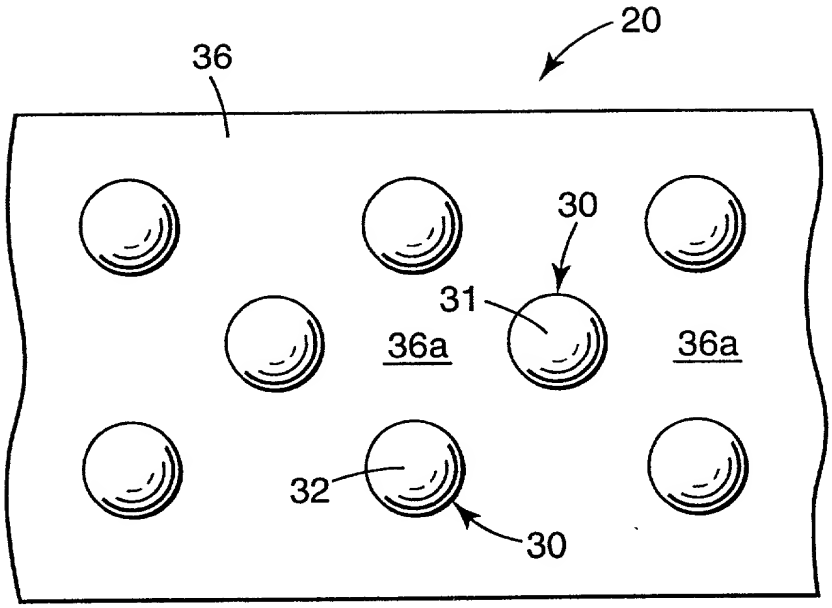

Fig. 2

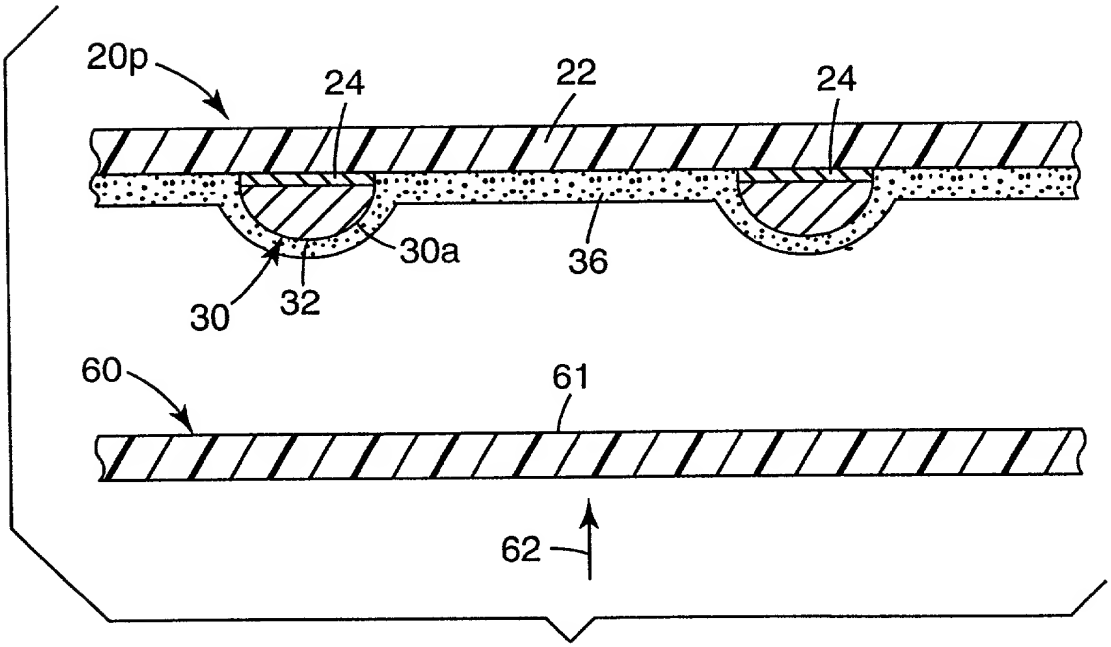

Fig. 3a

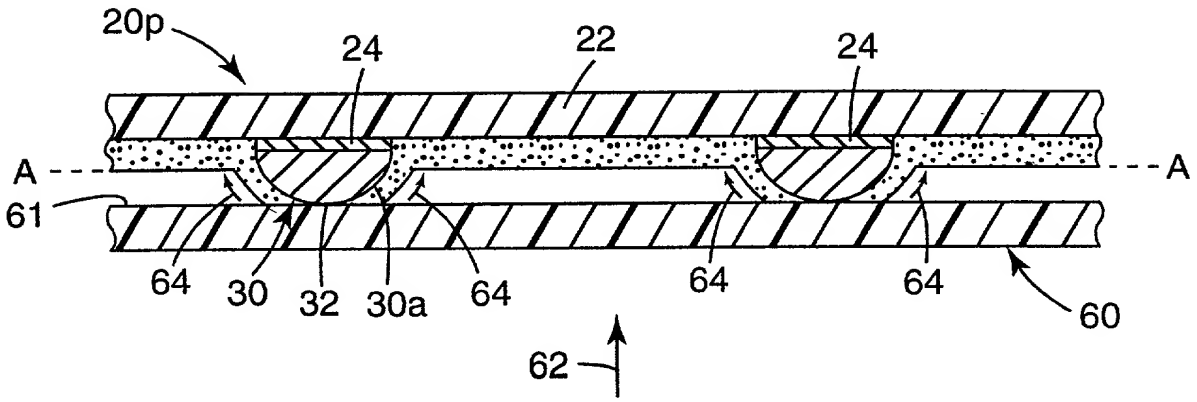
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Fig. 3b

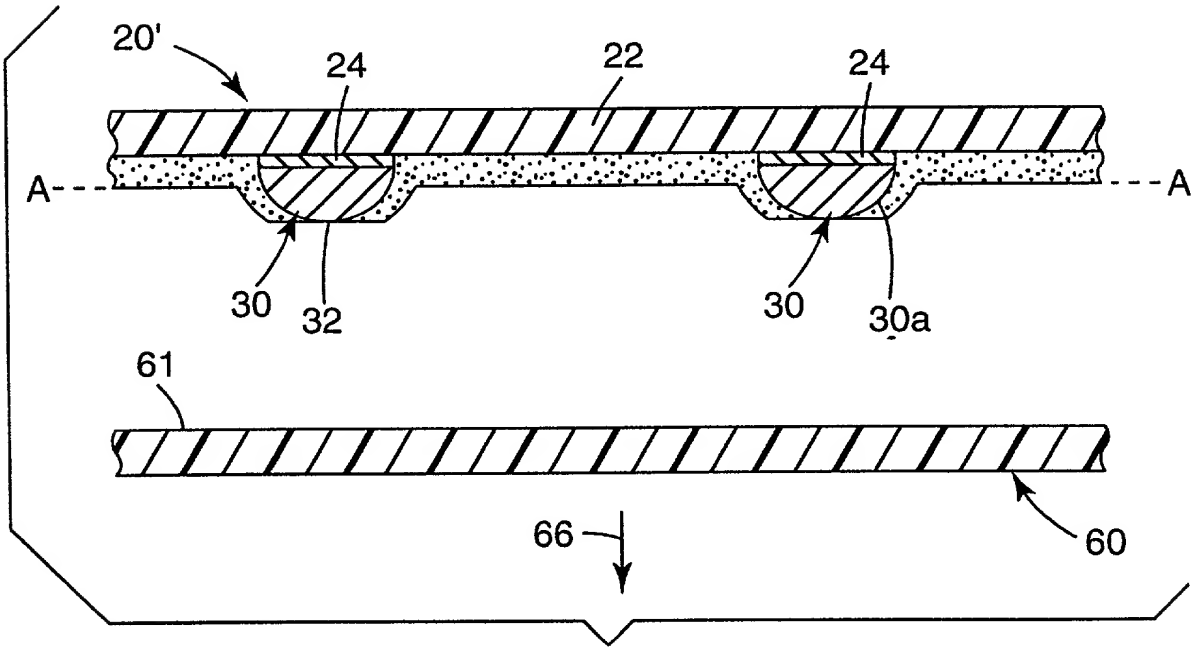
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Fig. 3c

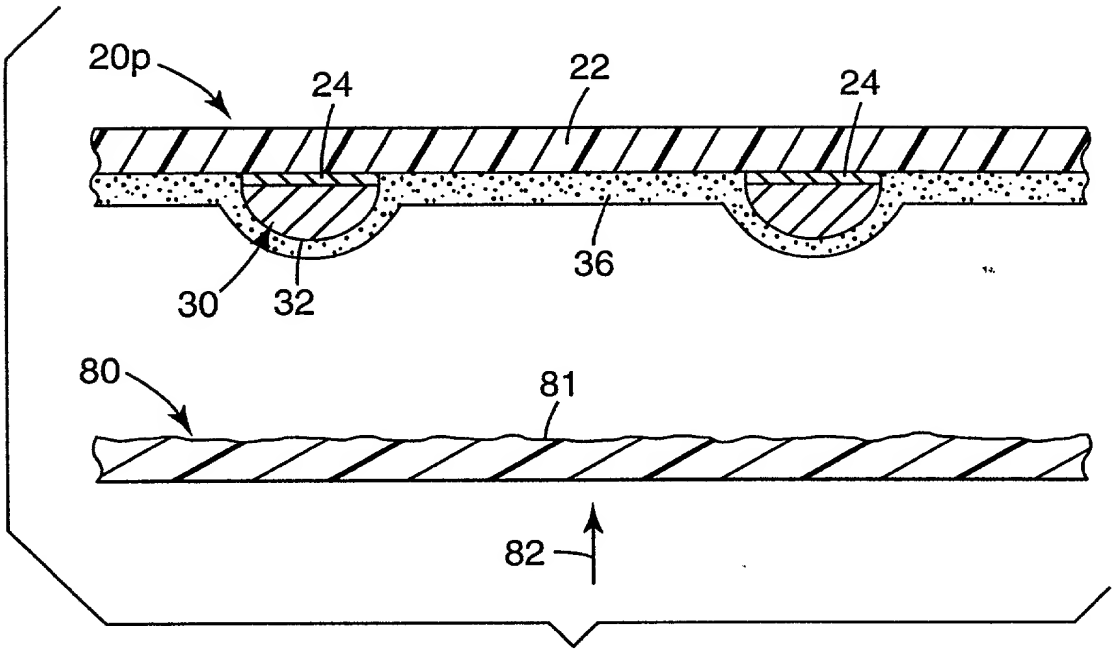

Fig. 4a

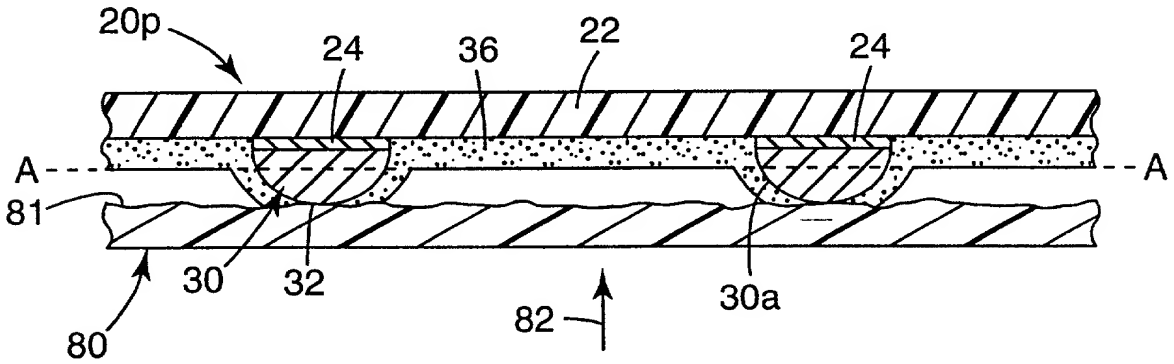

Fig. 4b

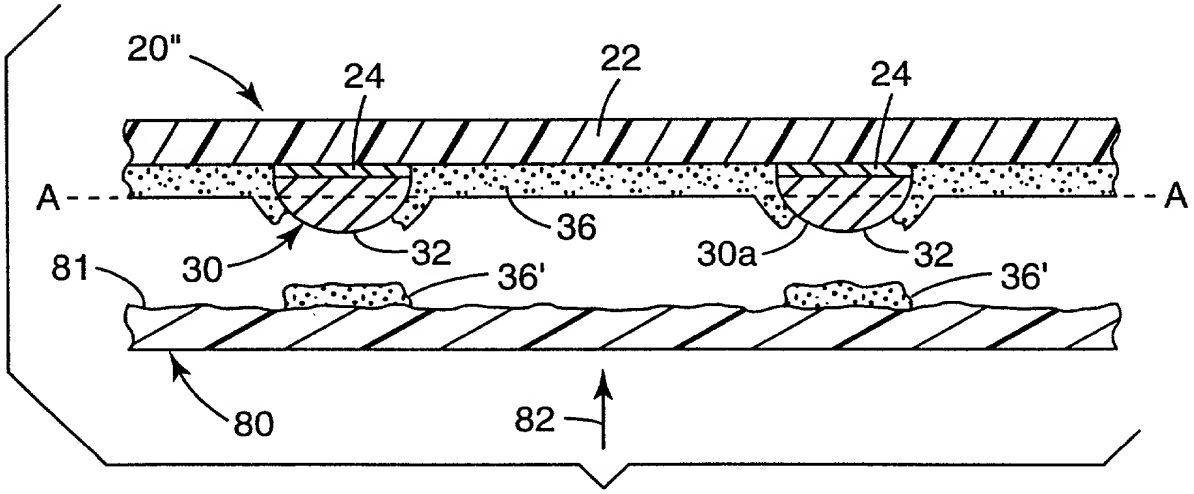

Fig. 4c

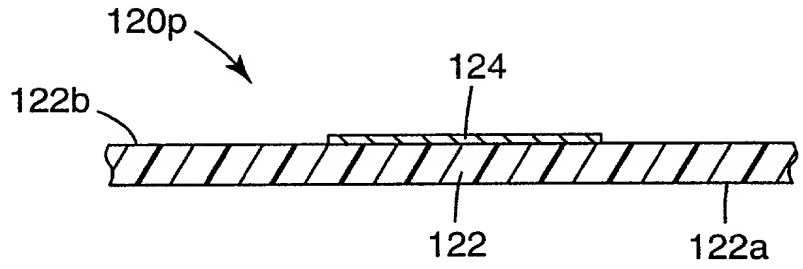

Fig. 5a

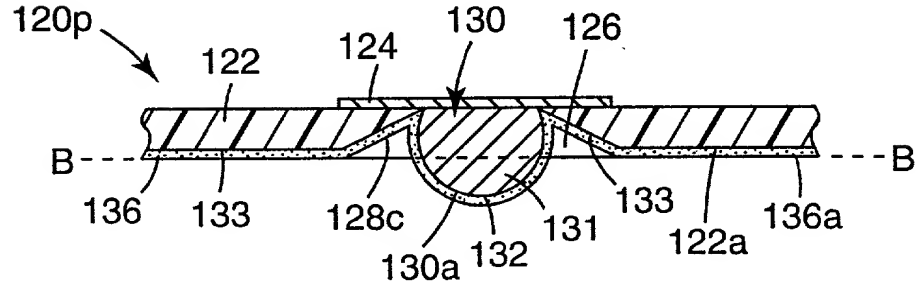

Fig. 5b

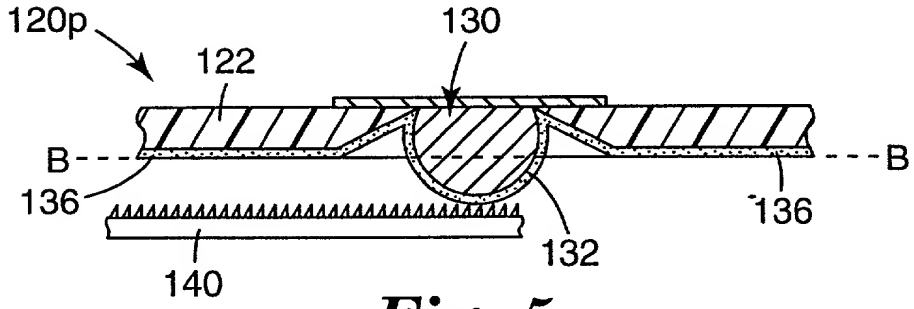

Fig. 5c

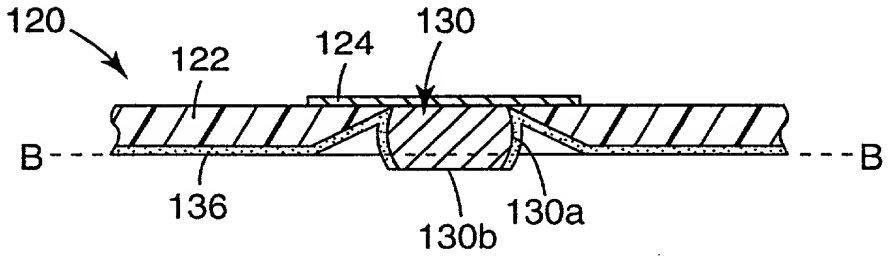

Fig. 5d

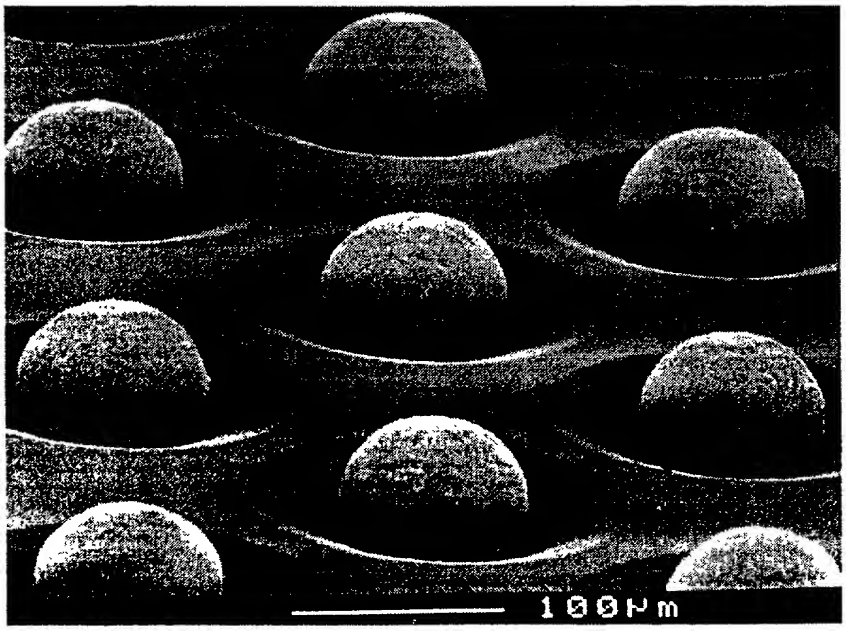

FIG.6A

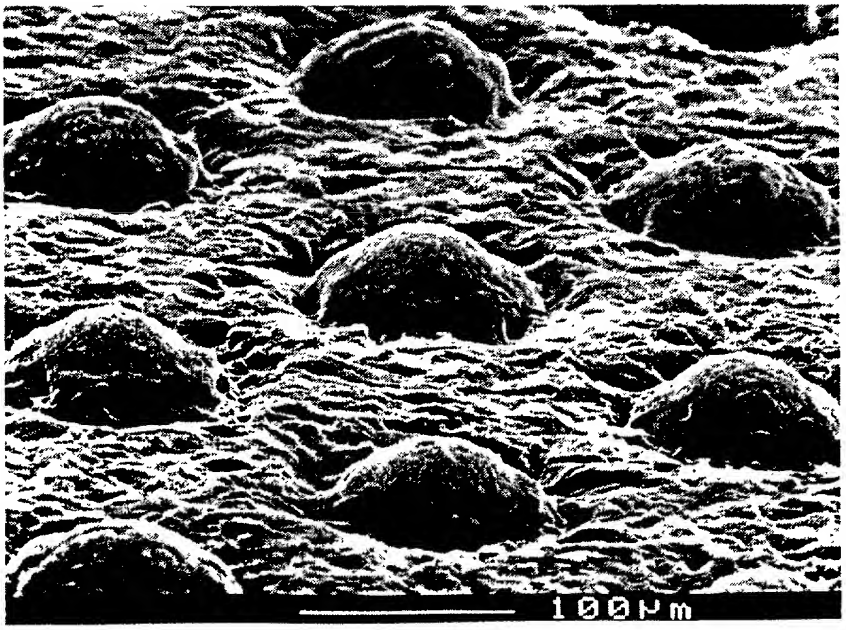

FIG.6B

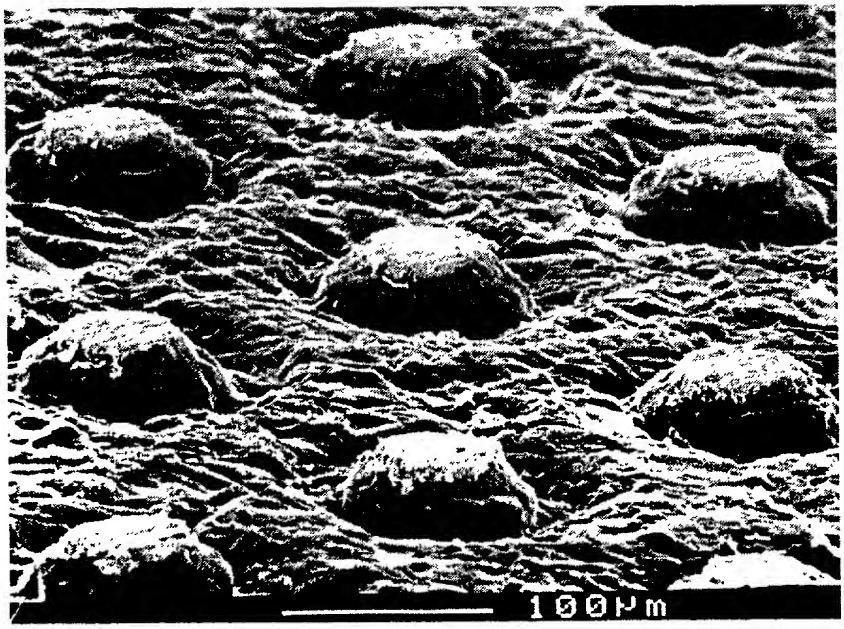

FIG.6C

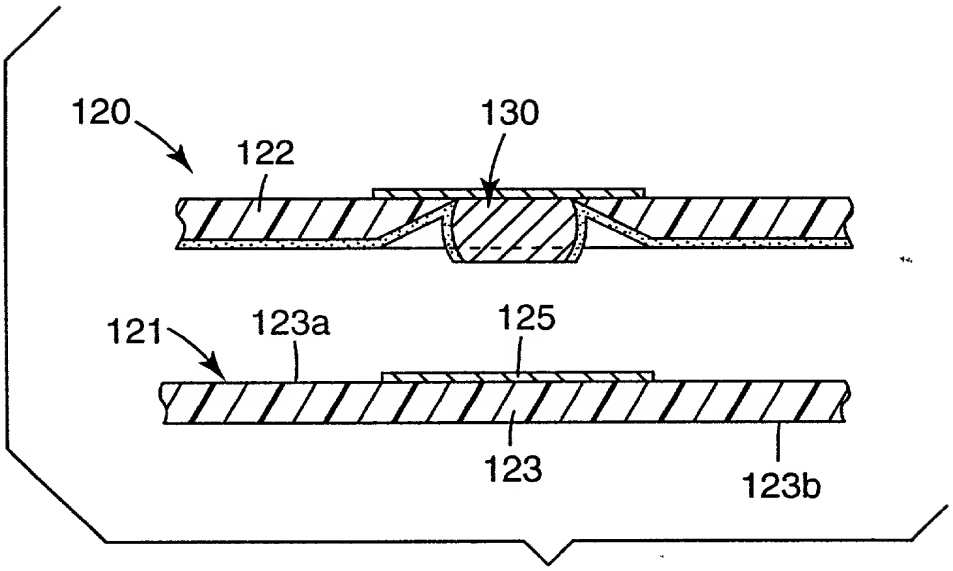

Fig. 5e

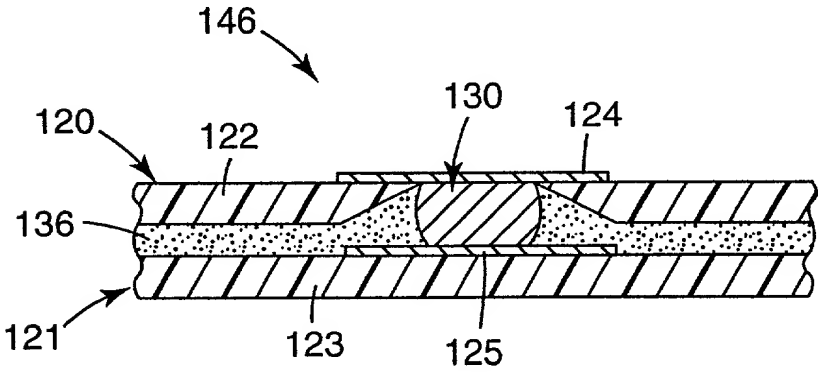

Fig. 5f

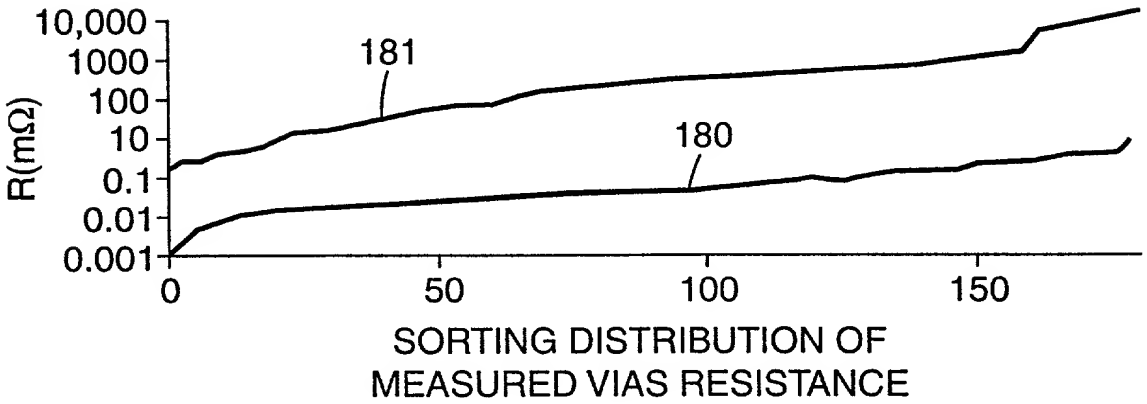

Fig. 7

Docket No. 52779USA3A

DECLARATION, POWER OF ATTORNEY, AND PETITION

I, a below named inventor, depose and say that: (1) my residence, citizenship, and mailing address are indicated below; (2) I have reviewed and understand the contents of my patent application, including the claims, as amended by any amendment specifically referred to herein, which is identified as U.S. Patent Application Serial No. 08/986882, filed December 8, 1997; (3) I believe that the other below named inventors and I are the original, first, and joint inventors or discoverers of the invention or discovery in

METHOD FOR MAKING CIRCUIT ELEMENTS FOR A Z-AXIS INTERCONNECT

described and claimed therein and for which a patent is sought; and (4) I hereby acknowledge my duty to disclose to the Patent and Trademark Office all information known to me to be material to the patentability as defined in Title 37, Code of Federal Regulations, §1.56.*

I hereby appoint Gregory D. Allen (Reg. No. 35,048), Scott A. Bardell (Reg. No. 39,594), Stephen W. Bauer (Reg. No. 32,192), Dale A. Bjorkman (Reg. No. 33,084), Jennie G. Boeder (Reg. No. 28,952), William J. Bond (Reg. No. 32,400), Warren R. Bovee (Reg. No. 26,434), Stephen W. Buckingham (Reg. No. 30,035), John A. Burtis (Reg. No. 39,924), Paul W. Busse (Reg. No. 32,403), Gerald F. Chernivec (Reg. No. 26,537), James D. Christoff (Reg. No. 31,492), David R. Cleveland (Reg. No. 29,524), Philip Y. Dahl (Reg. No. 36,115), Janice L. Dowdall (Reg. No. 31,201), Lisa M. Fagan (Reg. No. P-40,601), John A. Fortkort (Reg. No. 38,454), Richard Francis (Reg. No. 25,393), Gary L. Griswold (Reg. No. 25,396), Doreen S. L. Gwin (Reg. No. 35,580), H. Sanders Gwin (Reg. No. 33,242), Michaele A. Hakamaki (Reg. No. 40,011), Karl G. Hanson (Reg. No. 32,900), Nester F. Ho (Reg. No. 39,460), Jeffrey J. Hohenshell (Reg. No. 34,109), Robert W. Hoke (Reg. No. 29,226), John H. Hornickel (Reg. No. 29,393), MarySusan Howard (Reg. No. 38,729), Stephen C. Jensen (Reg. No. 35,207), Robert H. Jordan (Reg. No. 31,973), Walter N. Kirn, Jr. (Reg. No. 21,196), Harold C. Knecht III (Reg. No. 35,576), Charles D. Levine (Reg. No. 32,477), Douglas B. Little (Reg. No. 28,439), Eloise J. Maki (Reg. No. 33,418), John C. McFarren (Reg. No. 31,856), Matthew B. McNutt (Reg. No. 39,766), Michelle M. Michel (33,968), William D. Miller (Reg. No. 37,988), Darla P. Neaveill (Reg. No. 31,783), Peter L. Olson (Reg. No. 35,308), Daniel R. Pastirik (Reg. No. 33,025), David B. Patchett (Reg. No. 39,326), Carolyn V. Peters (Reg. No. 33,271), Terryl K. Qualey (Reg. No. 25,148), Ted K. Ringsred (Reg. No. 35,658), James A. Rogers (Reg. No. 37,228), Daniel C. Schulte (Reg. No. 40,160), Leland D. Schultz (Reg. No. 30,322), Steven E. Skolnick (Reg. No. 33,789), Robert W. Sprague (Reg. No. 30,497), James J. Trussel (Reg. No. 37,251), F. Andrew Ubel (Reg. No. 36,704), Lucy C. Weiss (Reg No. 32,834), my attorneys and/or agents with full powers (including the powers of appointment, substitution, and revocation) to prosecute this application and any division, continuation, continuation-in-part, reexamination, or reissue thereof, and to transact all business in the Patent and Trademark Office connected therewith; the mailing address and the telephone number of the above-mentioned attorneys and/or agents are

Attention: H. Sanders Gwin
3M Office of Intellectual Property Counsel
P.O. Box 33427
St. Paul, Minnesota 55133-3427
Telephone No. (612) 733-1500

The undersigned petitioner declares further that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Wherefore, I pray for grant of Letters Patent for the invention or discovery described and claimed in the aforementioned specification and we hereby subscribe our names to the foregoing specification and claims, declaration, power of attorney, and this petition, on the day set forth below.

5/13/98

Yu Chen — Date

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Joel A. Gerber 6/3/98
Date

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Brian E. Schreiber 5/13/98
Date

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Joshua W. Smith 2/19/98
Date

Joshua W. Smith
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§1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.